

Foxconn MCP61M07


Fab :A

nVIDIA MCP61 Chipset for AMD AM3 CPU

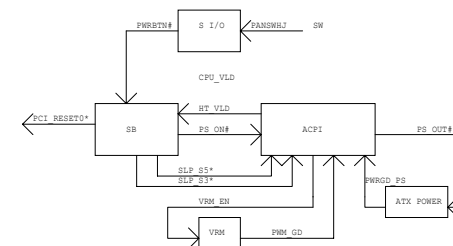
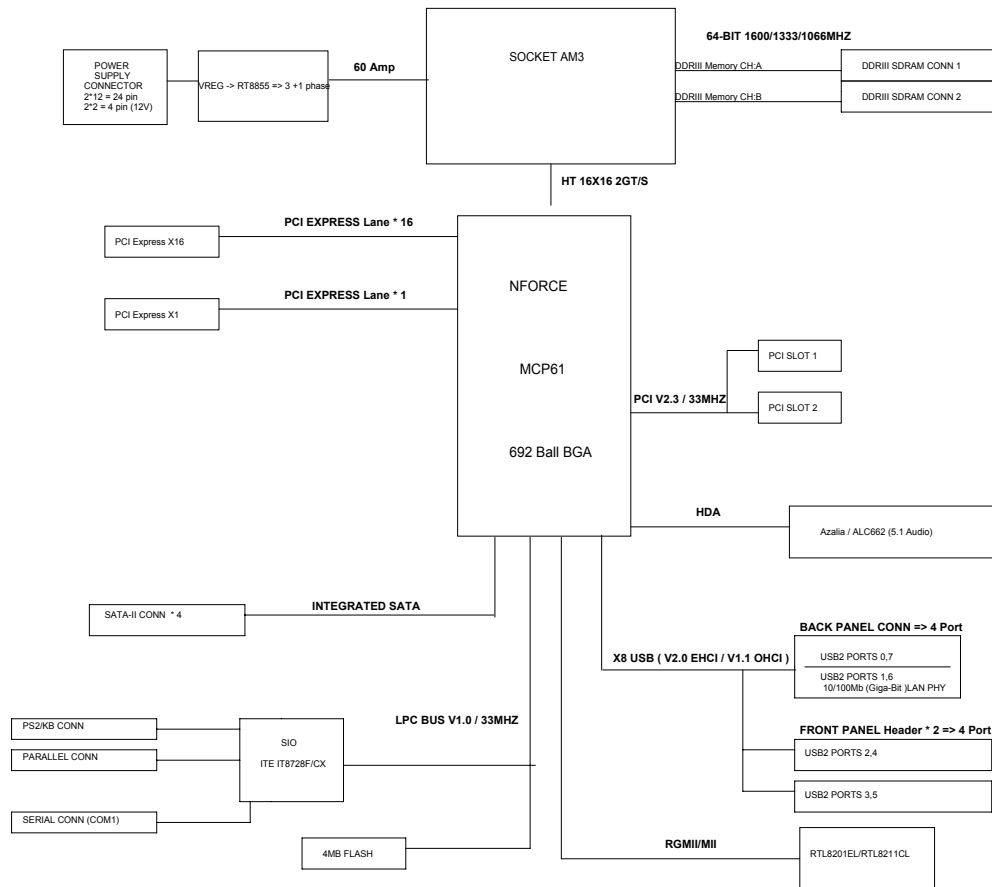
(12/04/2010)

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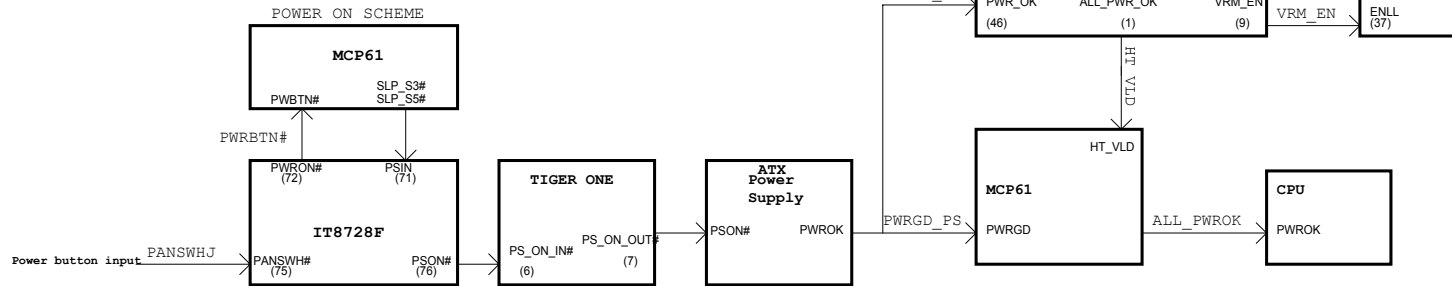
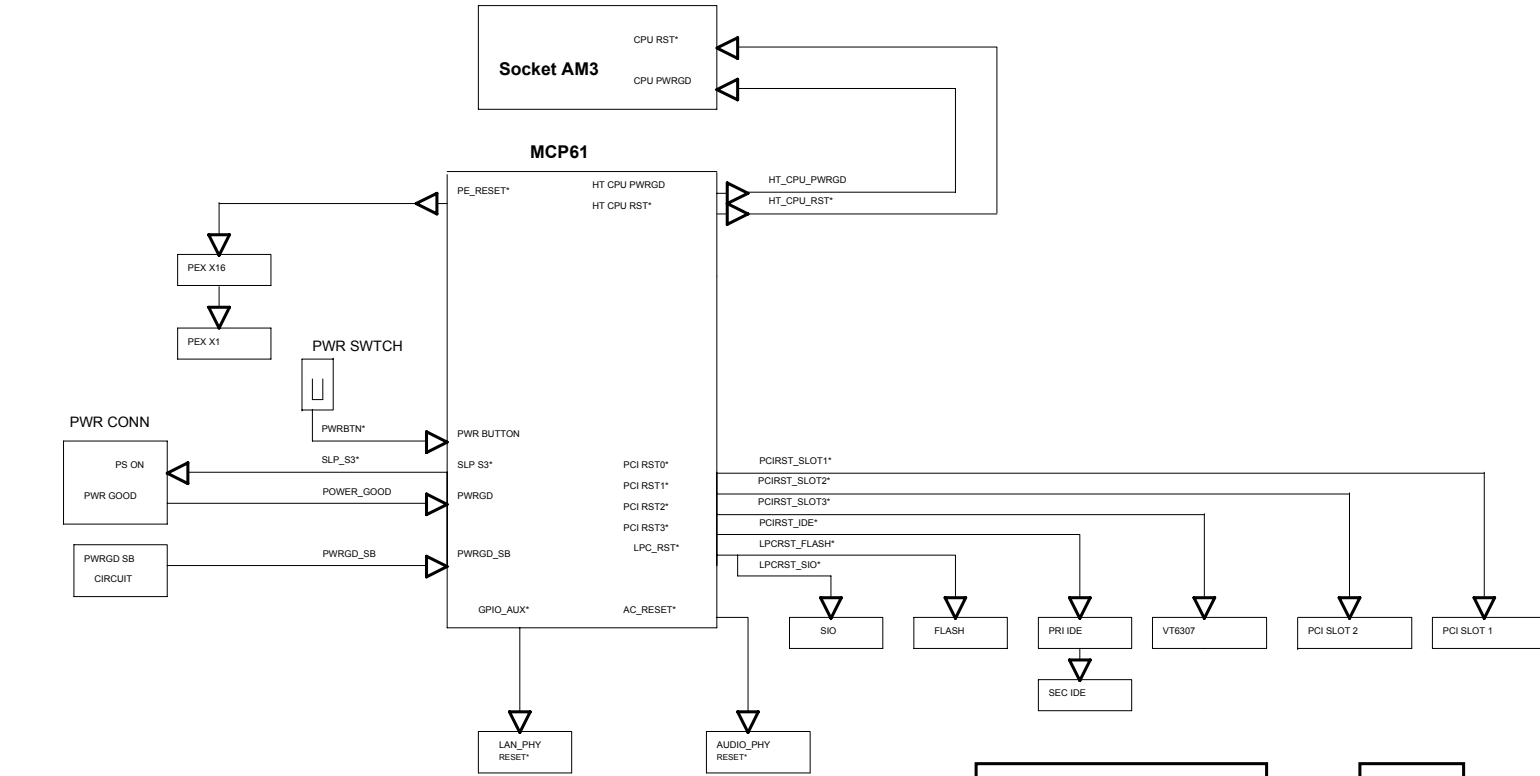
		
FOXCONN PCEG		
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Cover		
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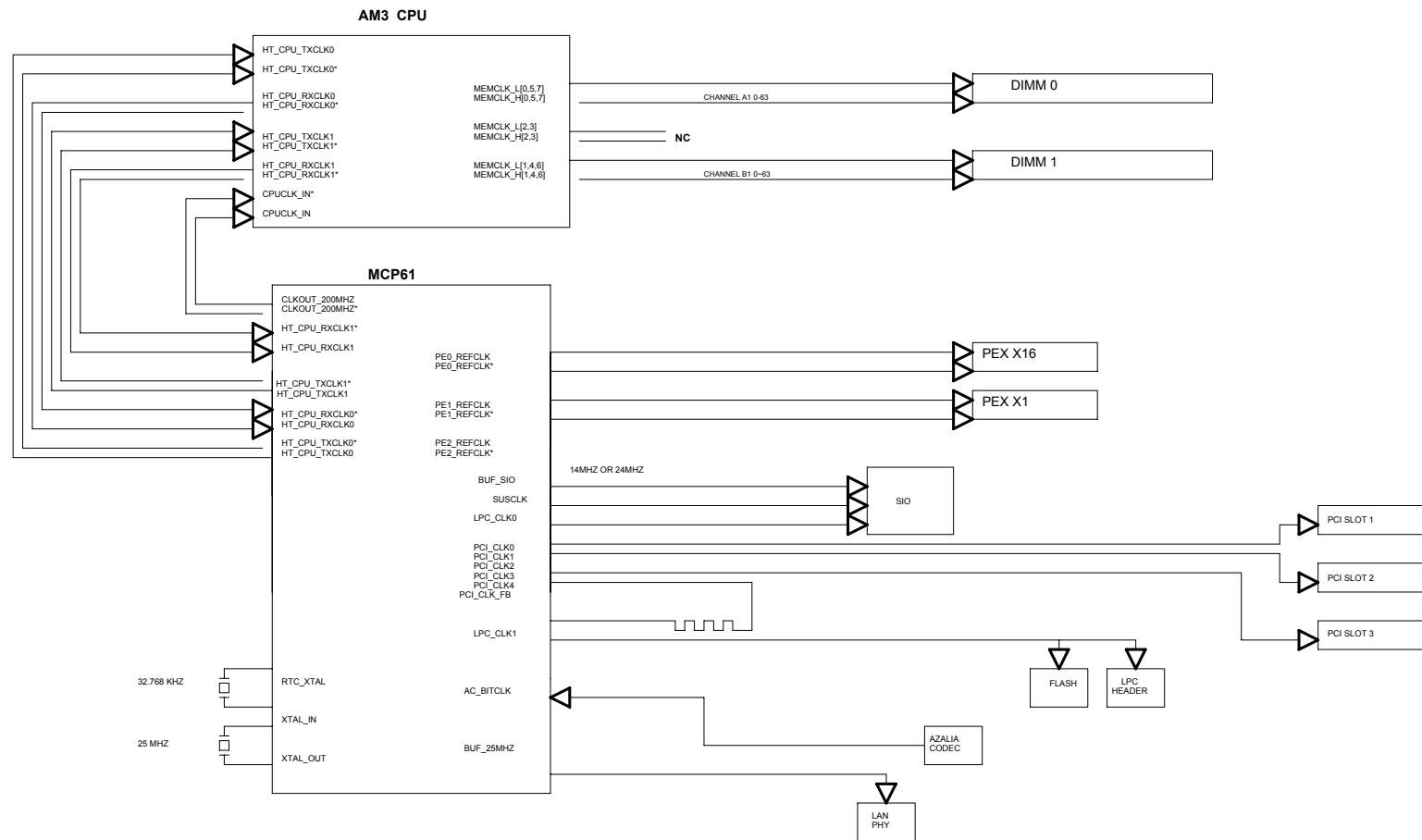
MCP61M07 Block Diagram



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RESET MAP





CPU VID TABLE			
VID [4..0]	VDD	VID [4..0]	VDD
0X00000	1.550V	0X10000	1.150V
0X00001	1.525V	0X10001	1.125V
0X00010	1.500V	0X10010	1.100V
0X00011	1.475V	0X10011	1.075V
0X00100	1.450V	0X10100	1.050V
0X00101	1.425V	0X10101	1.025V
0X00110	1.400V	0X10110	1.000V
0X00111	1.375V	0X10111	0.975V
0X01000	1.350V	0X11000	0.950V
0X01001	1.325V	0X11001	0.925V
0X01010	1.300V	0X11010	0.900V
0X01011	1.275V	0X11011	0.875V
0X01100	1.250V	0X11100	0.850V
0X01101	1.225V	0X11101	0.825V
0X01110	1.200V	0X11110	0.800V
0X01111	1.175V	0X11111	OFF

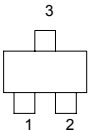
SMBUS ADDRESS MAP		
DEVICE	SMBUS #	ADDRESS
DIMM 0	0	1010 000 = 0X50
DIMM 1	0	1010 001 = 0X51
DIMM 2	0	1010 010 = 0X52
DIMM 3	0	1010 011 = 0X53
SIO	1	0101 101 = 0X2D
PCI SLOT 1	1	ARP
PCI SLOT 2	1	ARP
1394	1	ARP
DDC BUS	A	?
DDC BUS	B	?

PCI INTERRUPT/IDSEL MAP								
BACK PANEL SLOT	PCI BUS#	DEVICE#	IDSEL PIN	PCI SLOT INTA*	PCI SLOT INTB*	PCI SLOT INTC*	PCI SLOT INTD*	REQ/GNT
VT8308	01	0X06	22	P_INTZ*				1/1
PCI 2	01	0X08	23	P_INTW*	P_INTX*	P_INTY*	P_INTZ*	2/2
PCI 1	01	0X09	24	P_INTX*	P_INTY*	P_INTZ*	P_INTW*	3/3

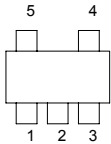
PCI DEVICE MAP

DEVICE	PCI BUS#	DEVICE#	FUNCTION	DEVICE ID
MCP 61	MCP61 LOGICAL PCI BUS 0	0X01-0X0F	--	--
MAC IMAC	0	XA	0	0X0057
PCI-PCI BRIDGE	0	X8	0	0X005C
SATA1	0	X8	0	0X0055
SATA0	0	X8	0	0X0054
IDE	0	X8	0	0X0053
MODEM CODEC	0	X4	1	0X0058
AUDIO CODEC	0	X4	0	0X0059
USB 2.0	0	X2	1	0X005B
USB 1.1	0	X2	0	0X005A
SHAPE TRIM	0	X1	2	0X005F
LDT	0	X0	0	0X005E
SMBUS2	0	X1	1	0X0052
LEGACY SLAVE	0	?	?	0X00D3
LPC	0	X1	0	0X0050/51
LOGICAL PCI BUS	1	?	?	?
PCI SLOT 1				
PCI SLOT 2				
PCI SLOT 3				
PCI SLOT 4				
PCI SLOT 5				

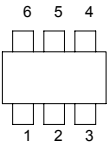
SOT23



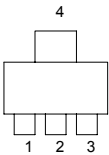
SOT23-5/SC70
SOT89-5



SOT23-6



SOT223

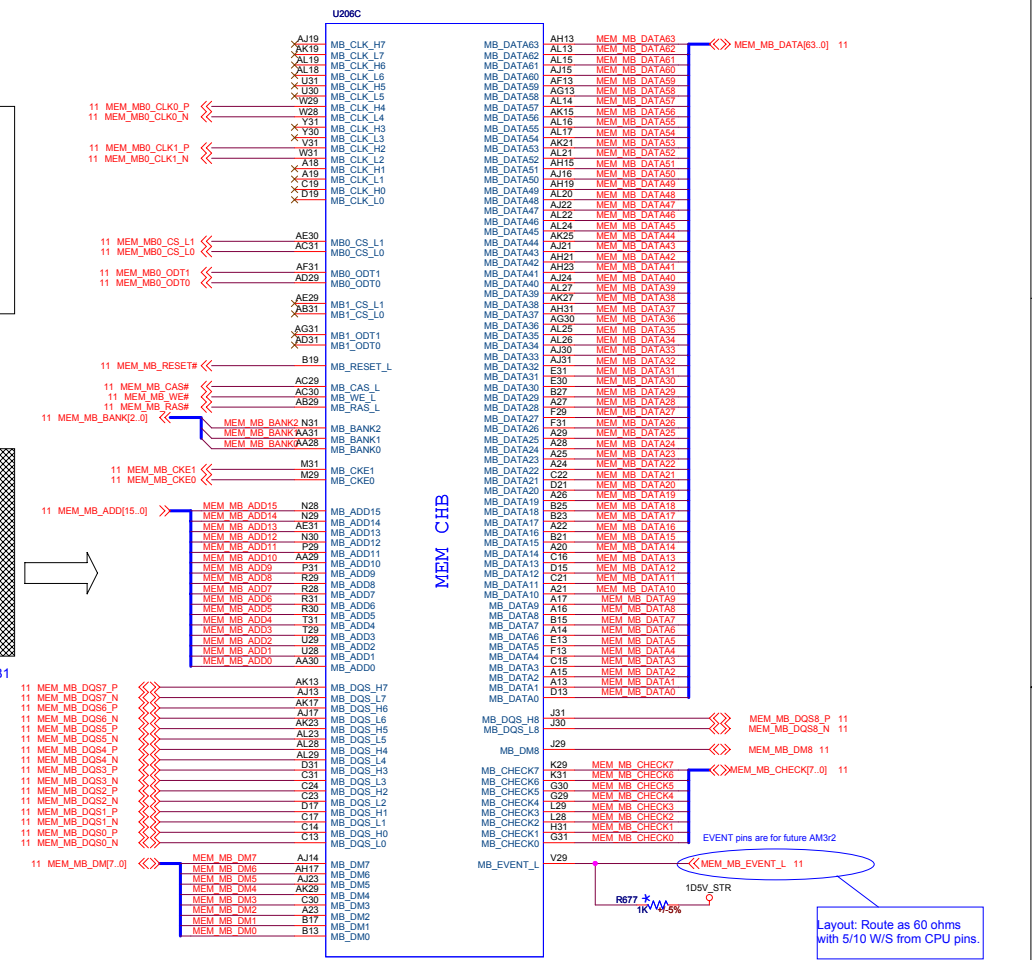
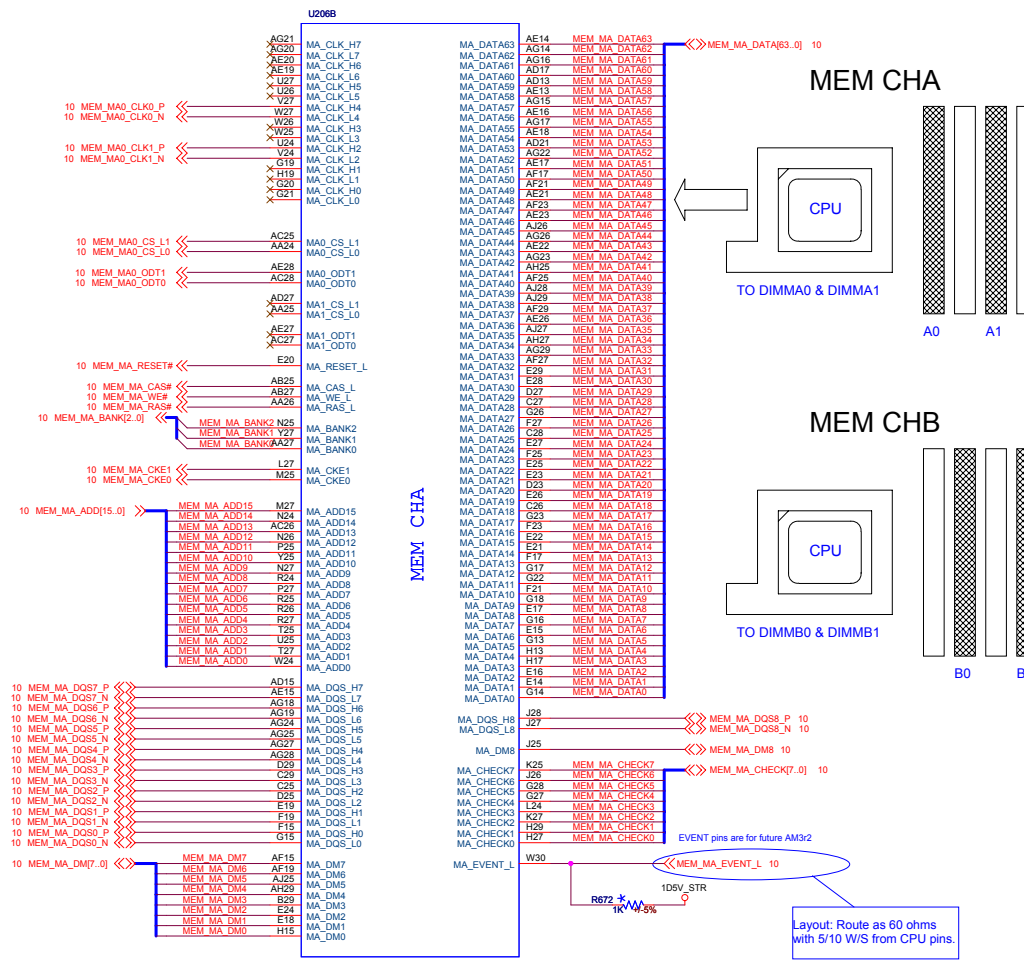


Title			
AM3 HyperTransport			
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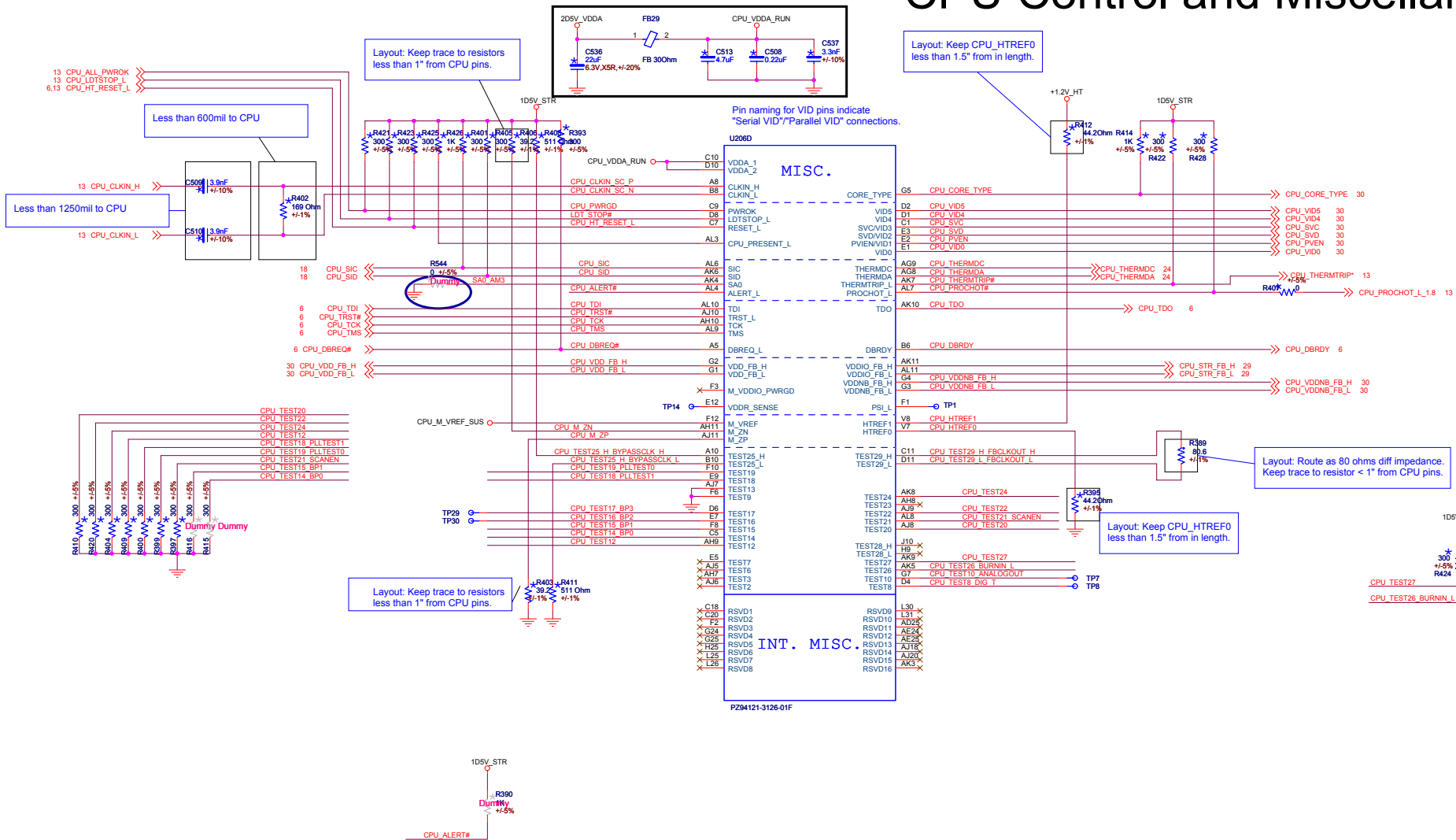
CPU Memory

DDR3 Memory Interface A

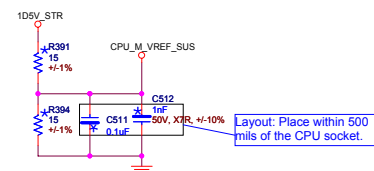
DDR3 Memory Interface B

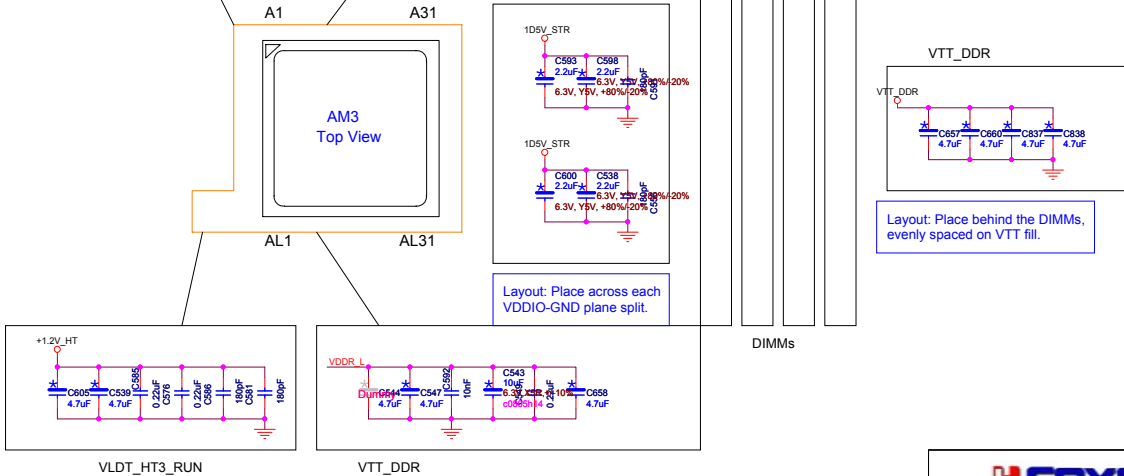
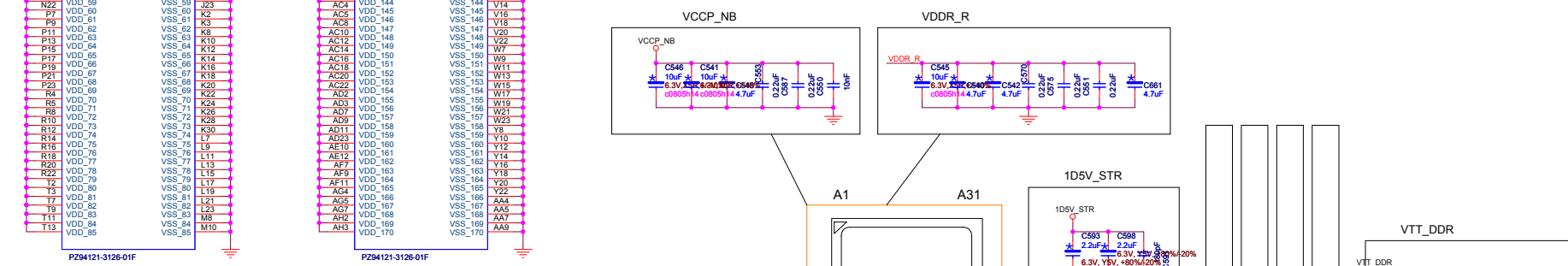


CPU Control and Miscellaneous

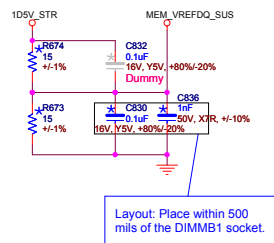


CPU_M_VREF_SUS

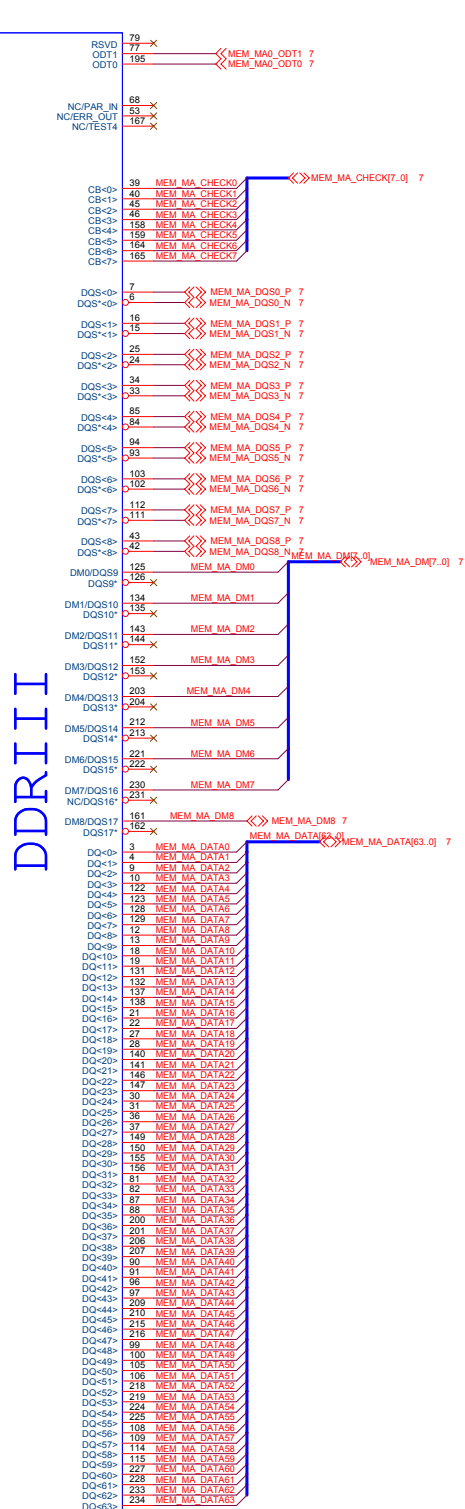
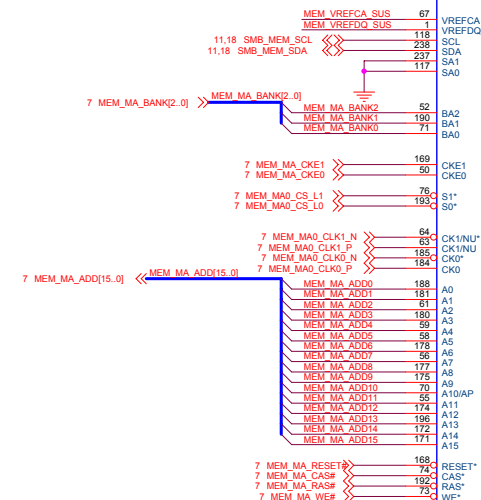
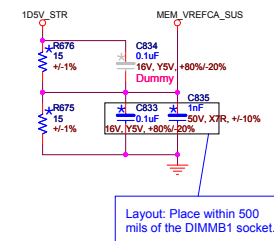




MEM_VREFDQ_SUS



MEM_VREFCA_SUS

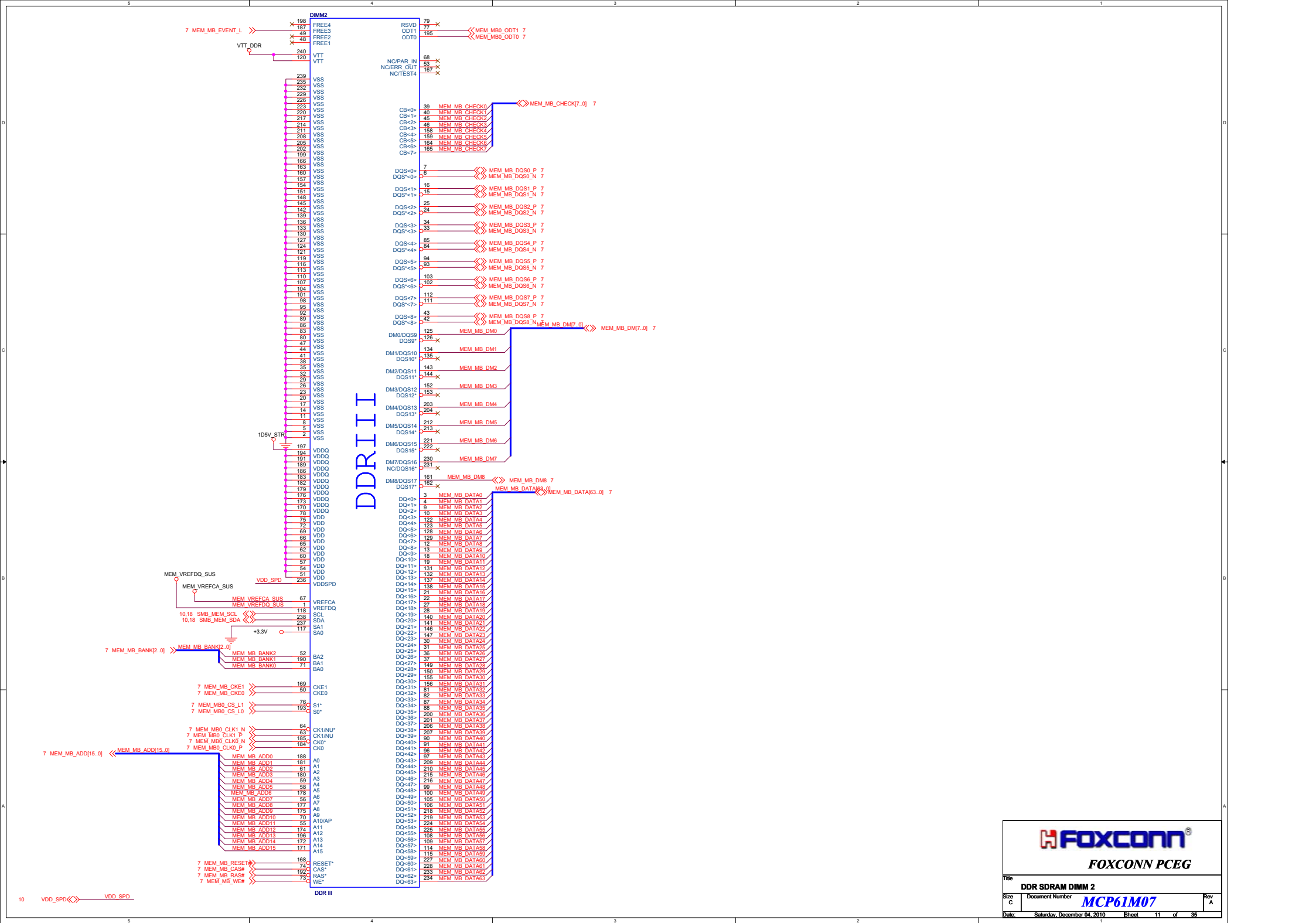


SMBus Addressing

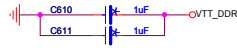
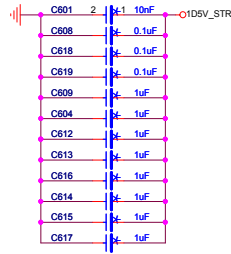
SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6



Title			
DDR SDRAM DIMM 1			
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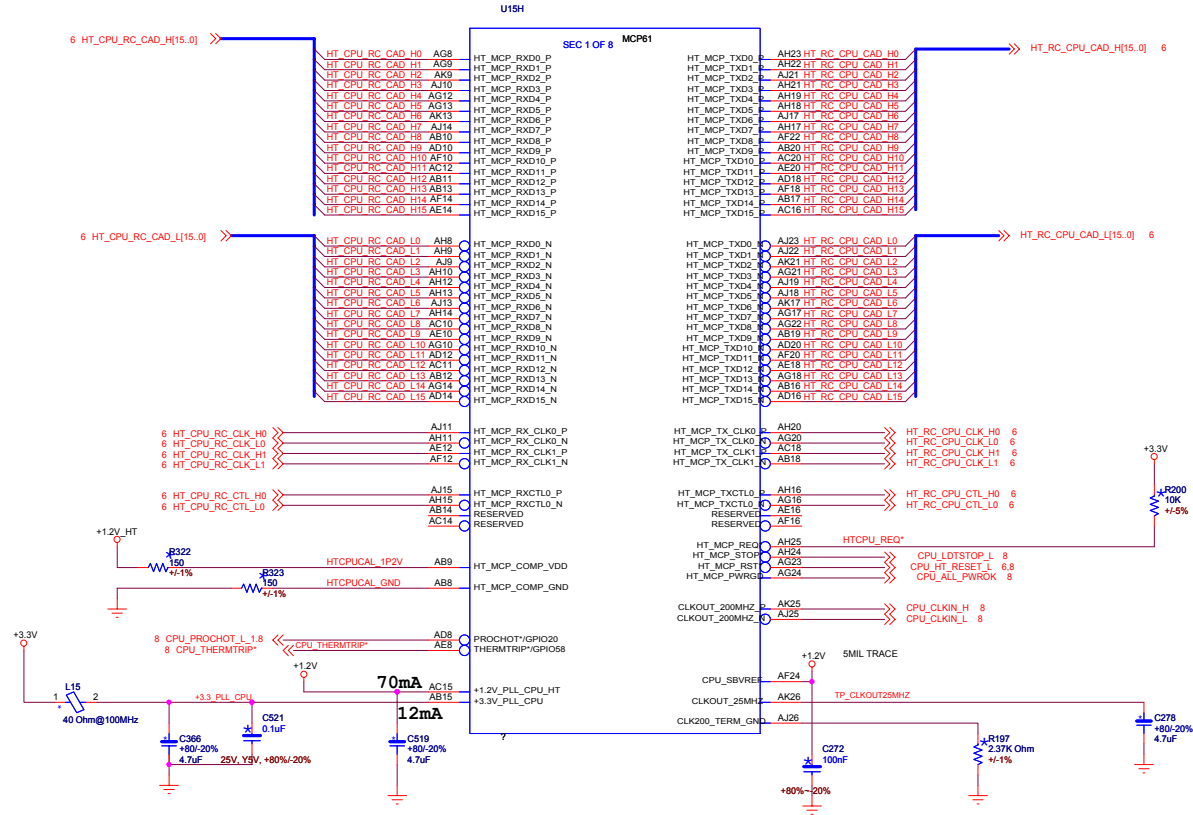


EMI decoupling cap. place evenly around 1D8V_STR

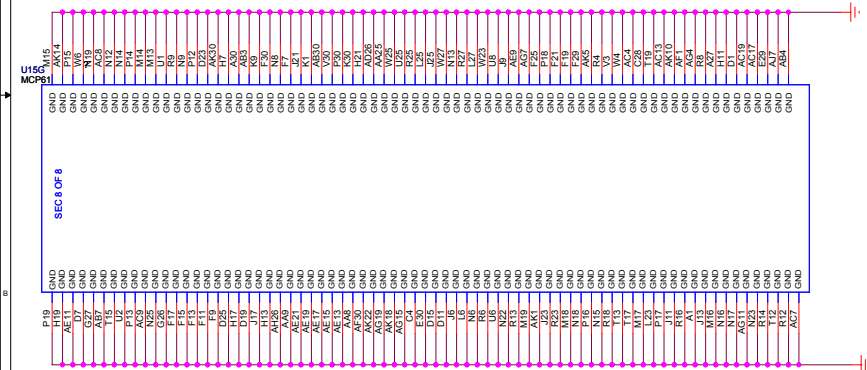
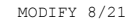


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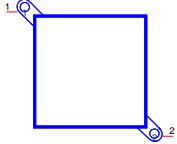
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DDR III terminator		
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MCP61 DECOUPLING

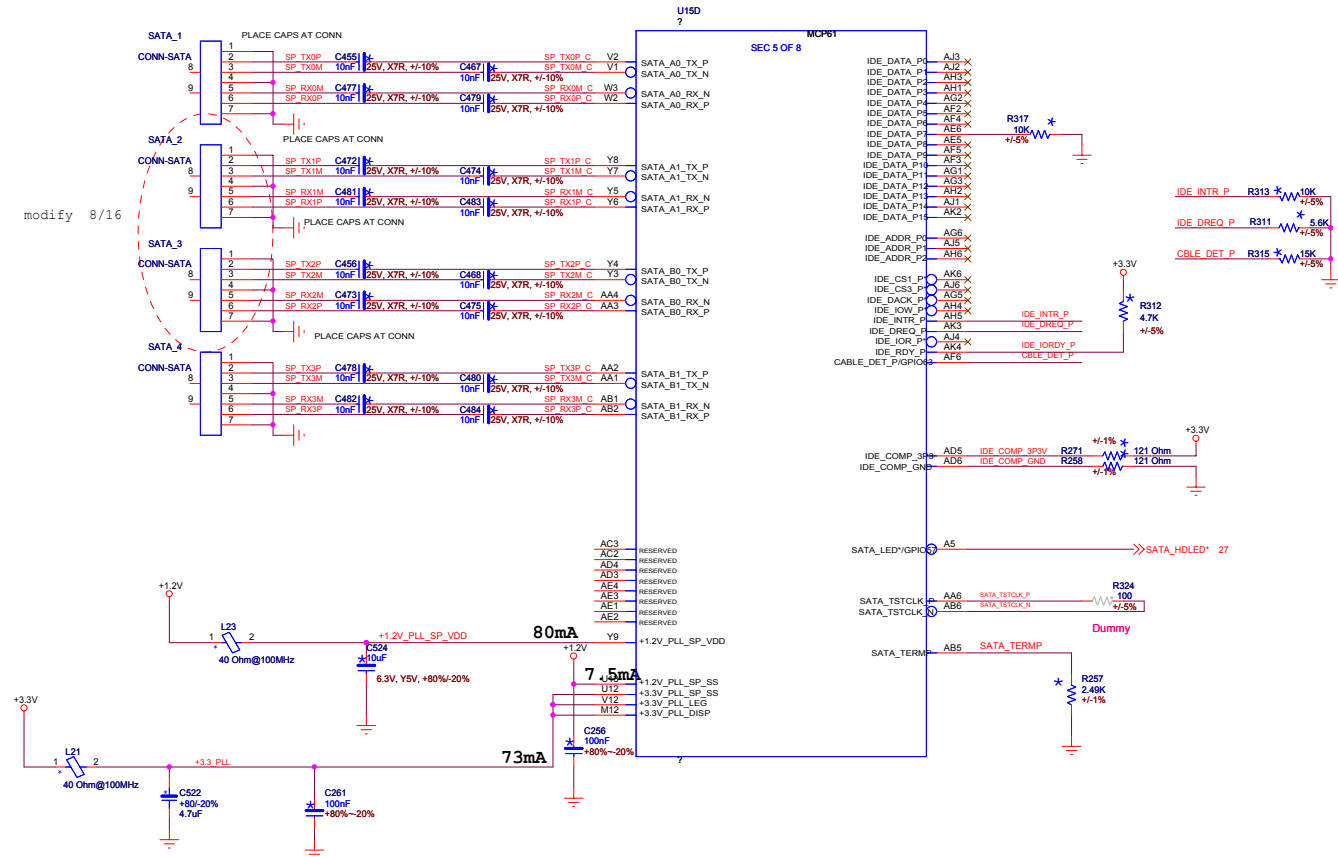


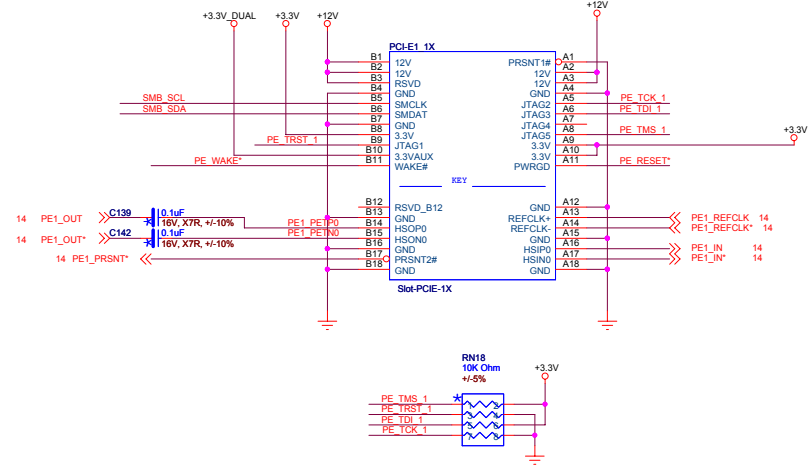
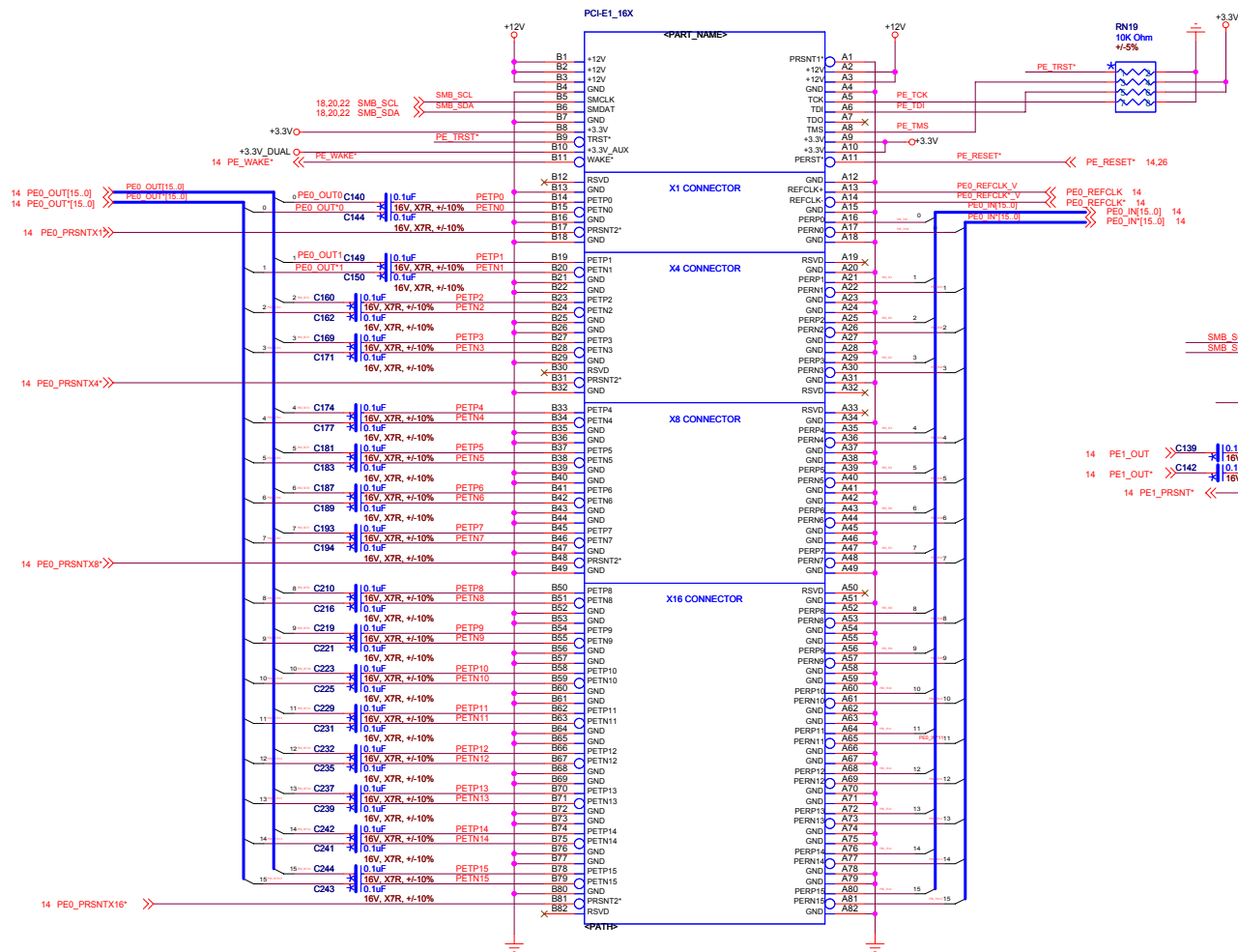
U15_1



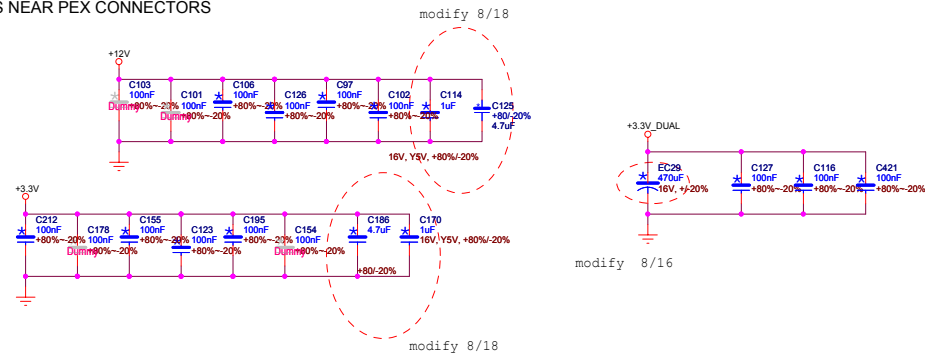
Heatsink_NB

modify 8/16



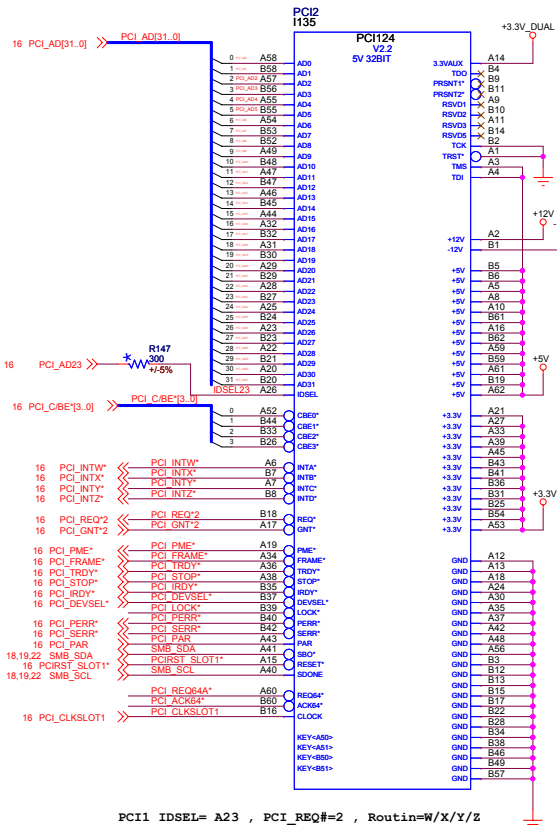


PLACE CAPS NEAR PEX CONNECTORS



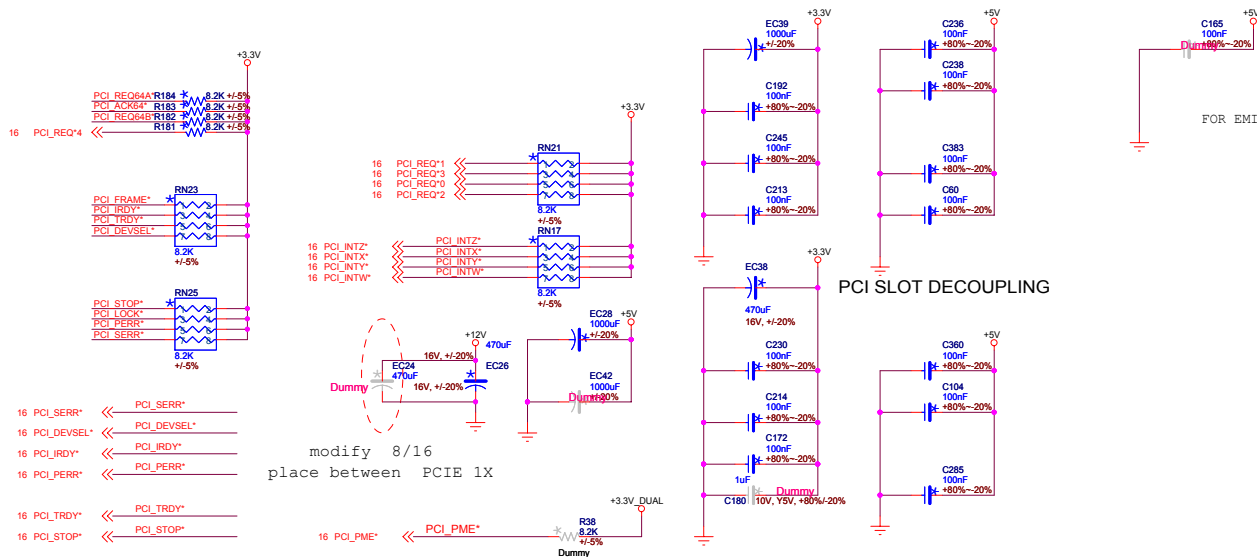
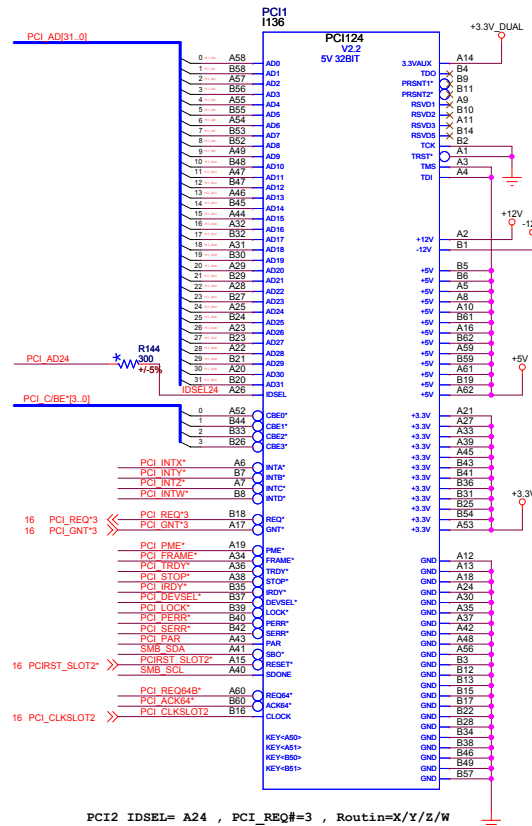
SLOT 2

IDSEL23

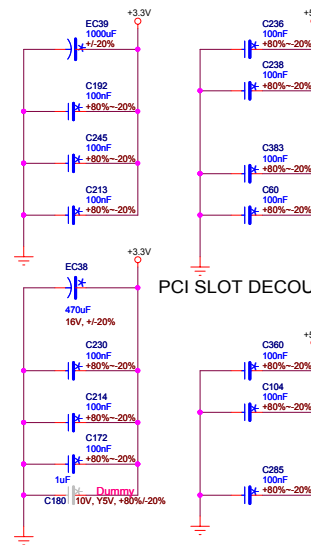


SLOT 1

IDSEL24



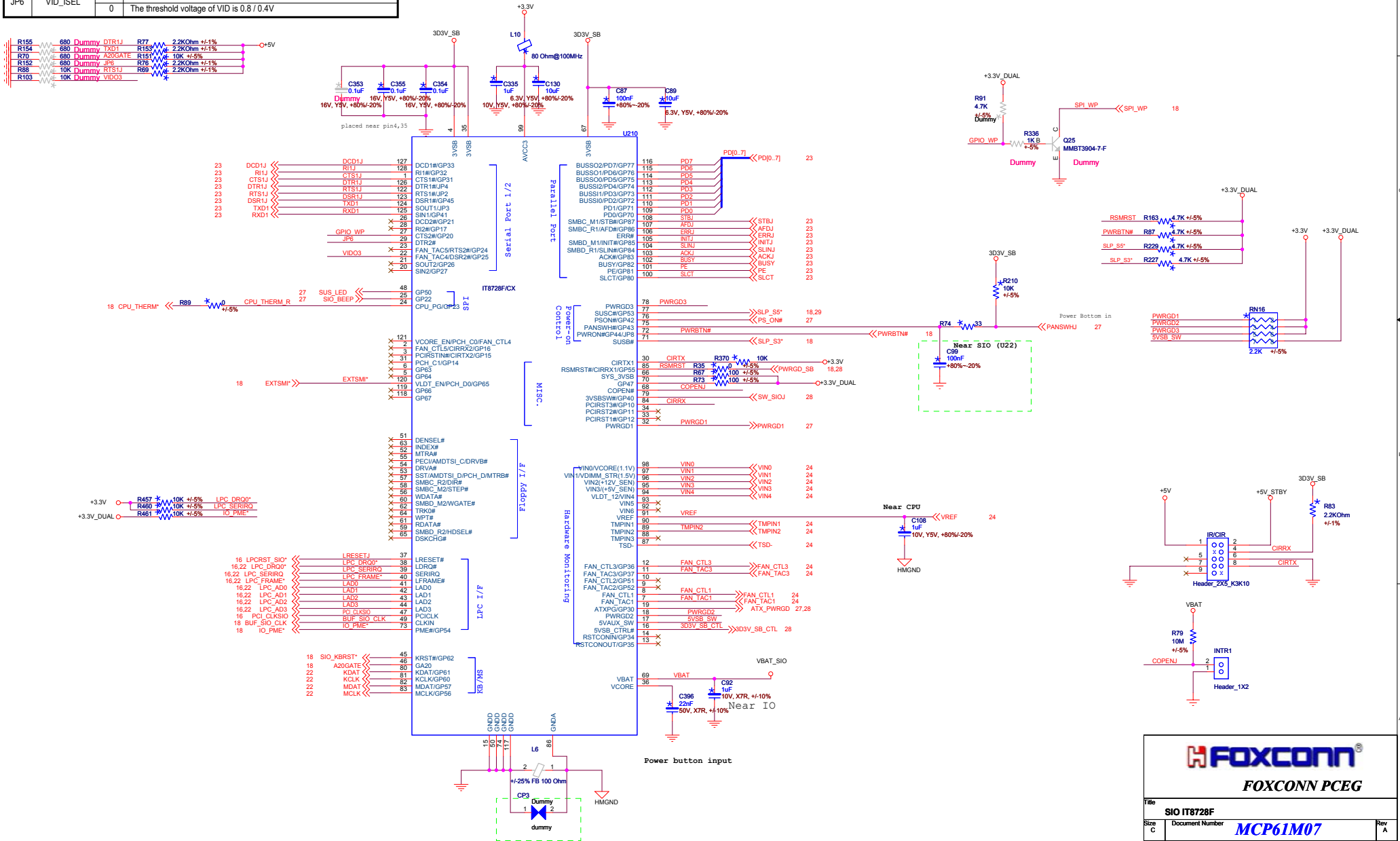
PCI SLOT DECOUPLING



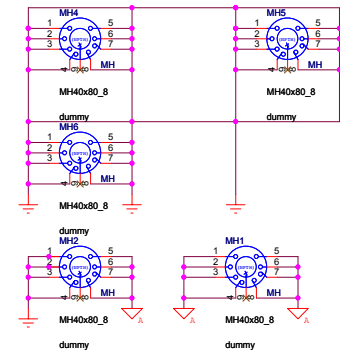
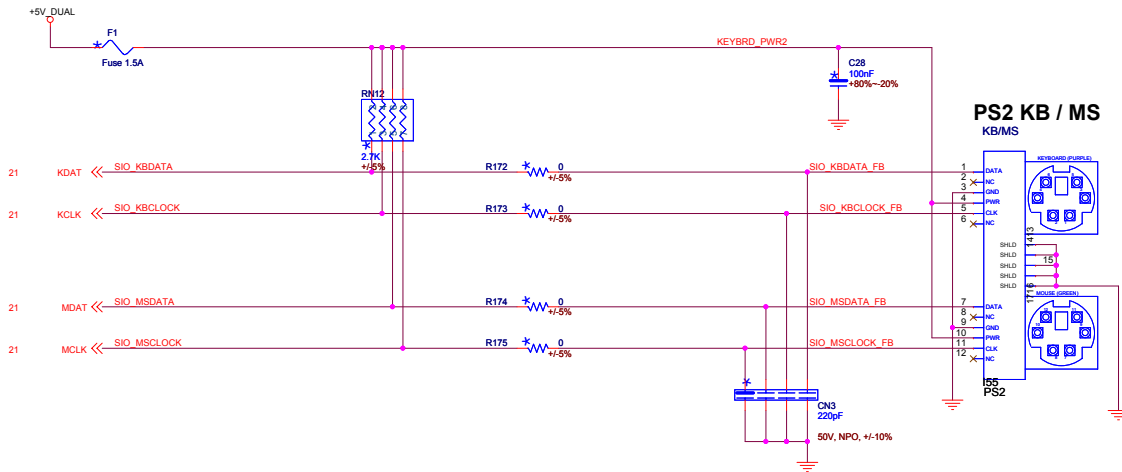
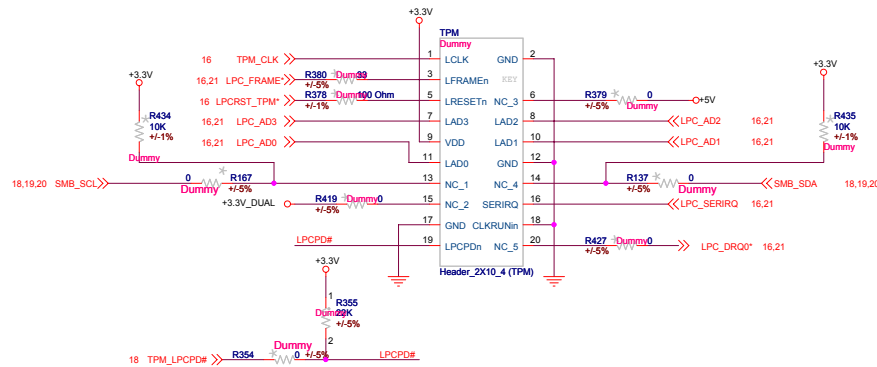
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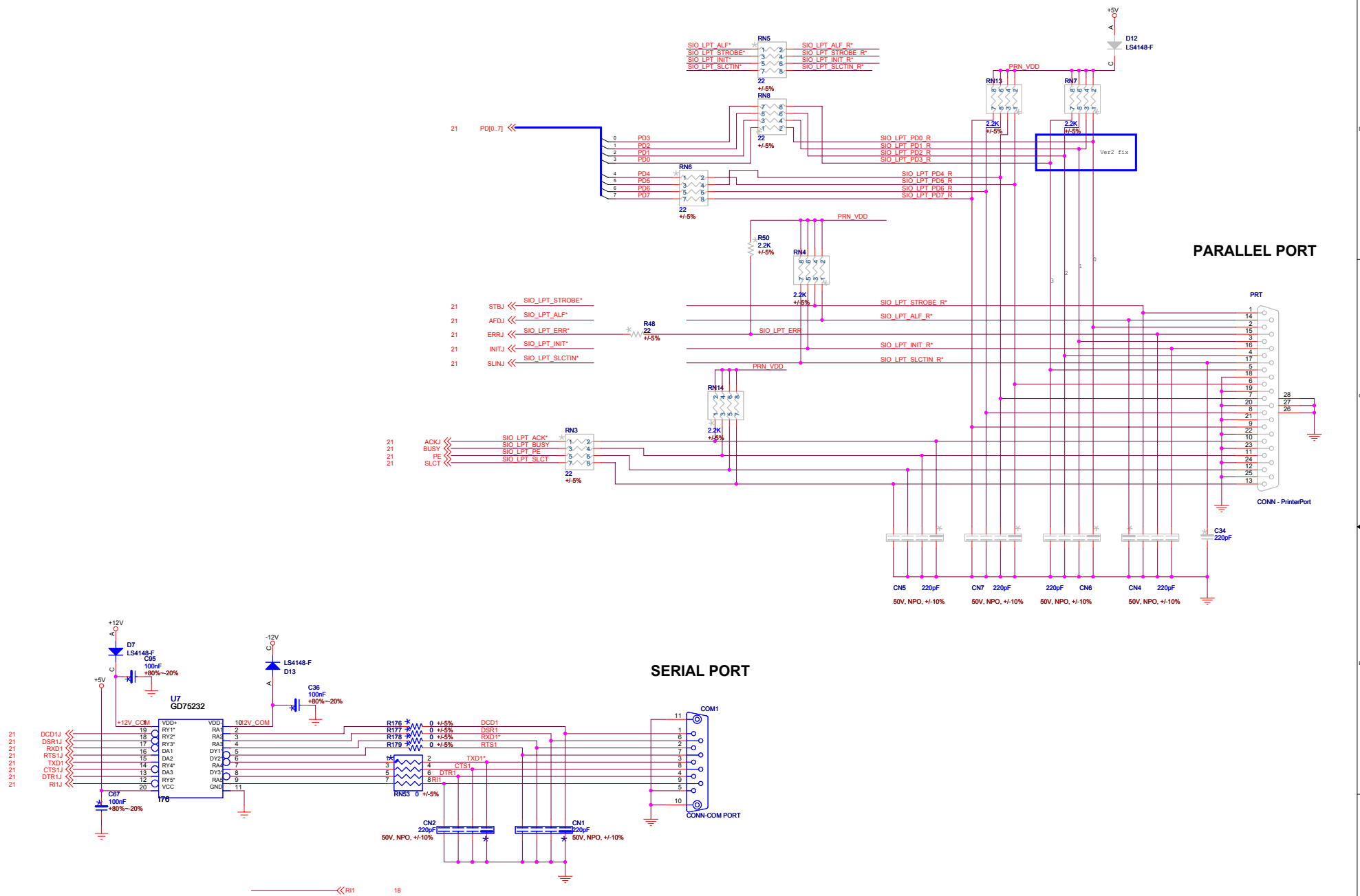
Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
JP2	SerFlh_SO_SEL	0	Flash I/F Address Segment 1 (FFFF_0000h~FFFF_FFFFh, 000F_0000h~000F_FFFFh) is enabled
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are open-drain.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

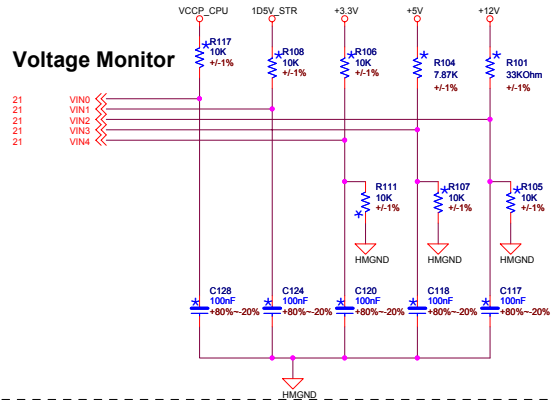


TPM Connector

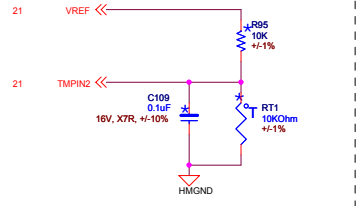
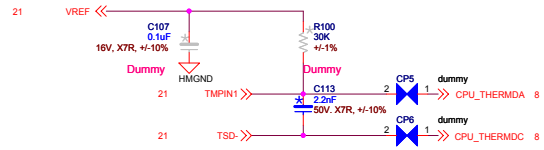




Voltage Monitor

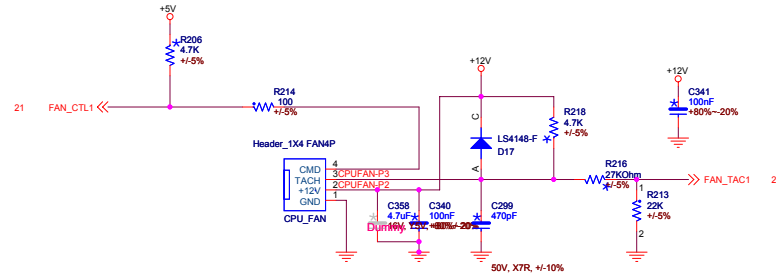


Thermal Controller

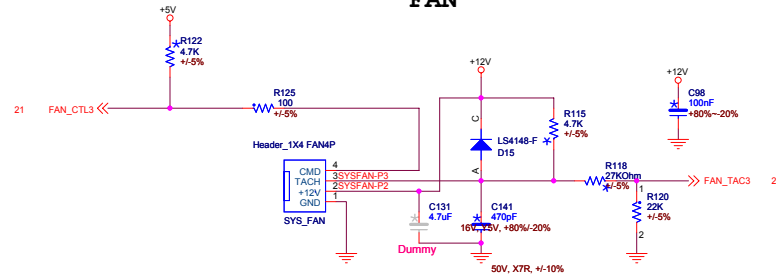


CPU FAN

New FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense
pin4. Control



SYSTEM FAN



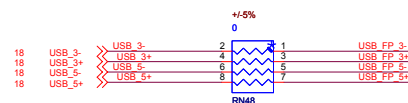
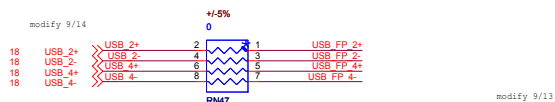
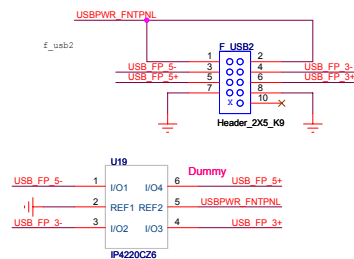
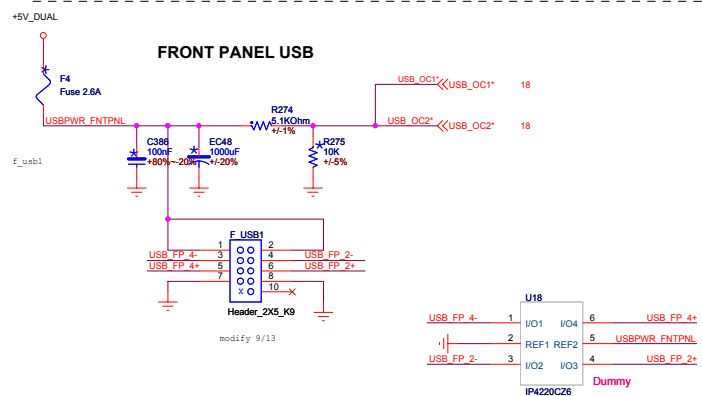
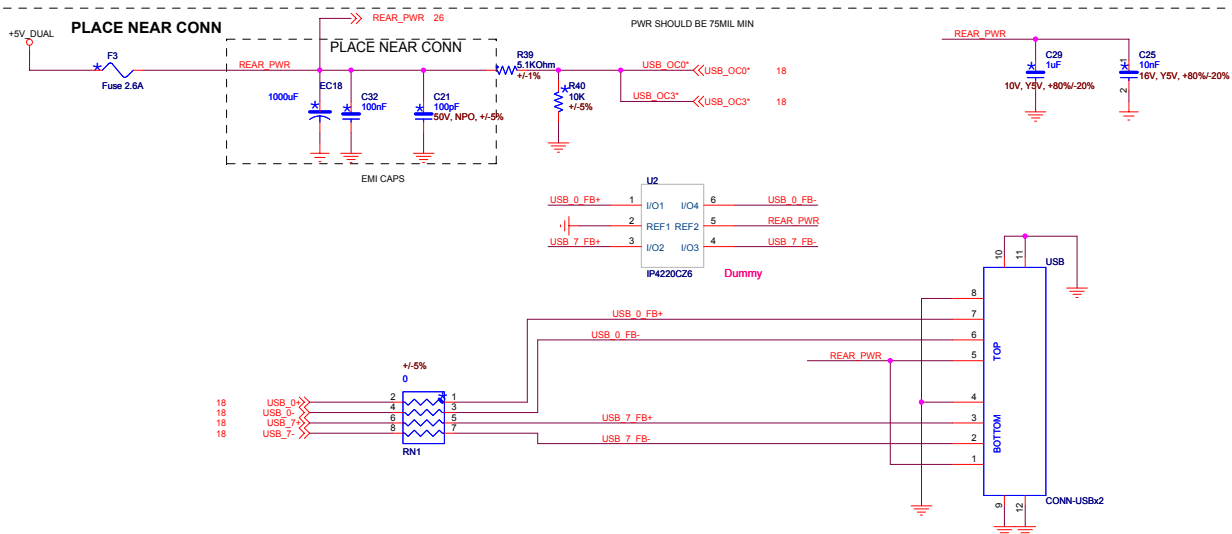
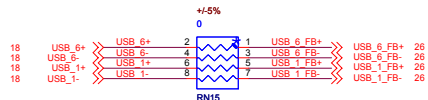
Need to check GPIO default
value at power-on .

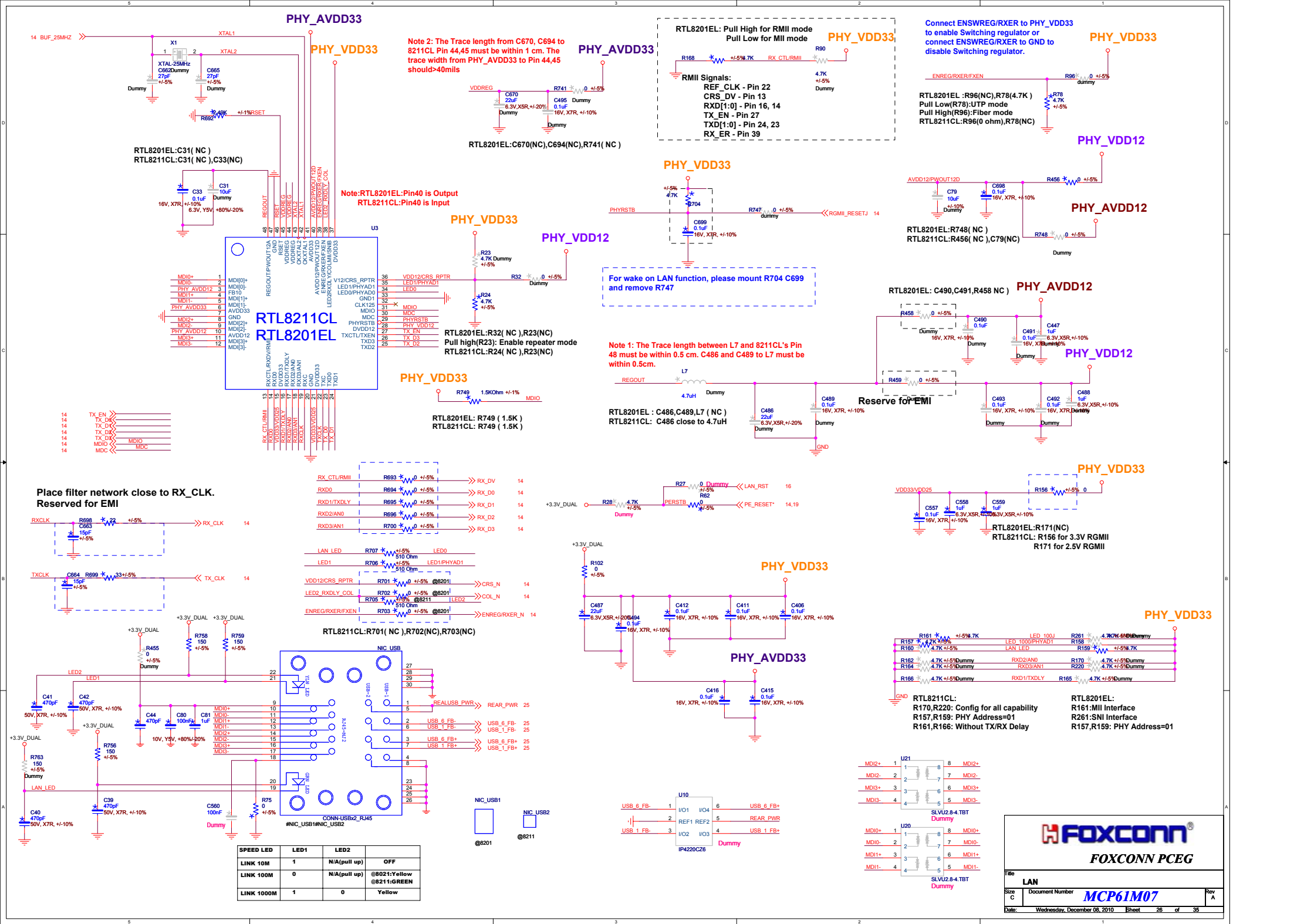
FOXCONN

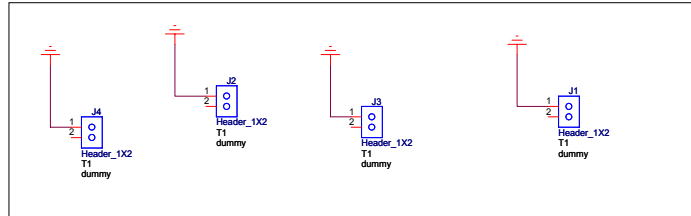
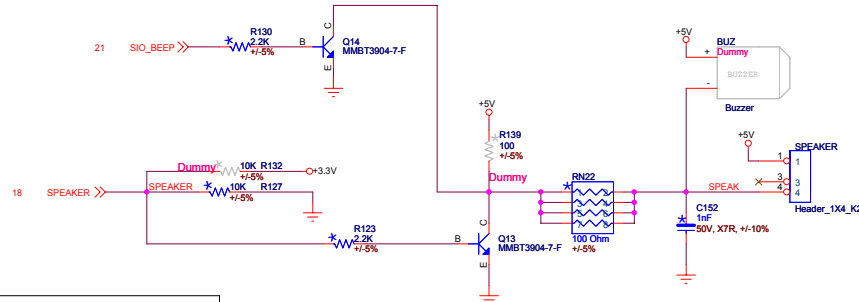
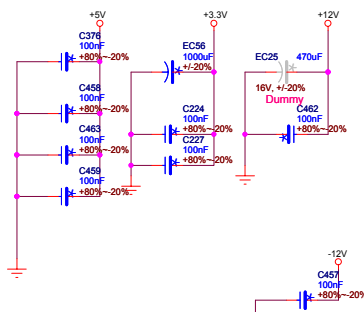
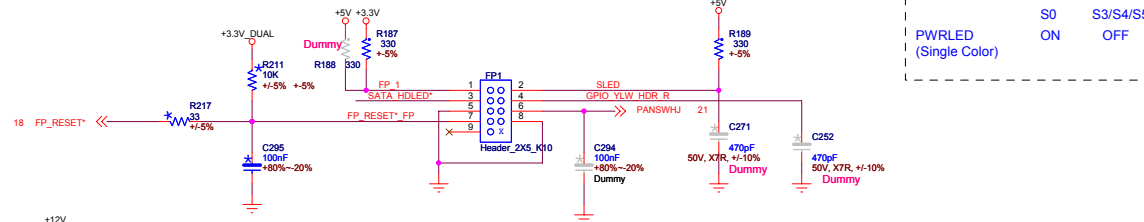
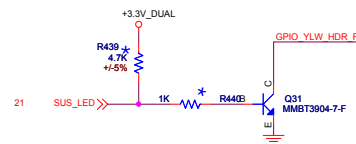
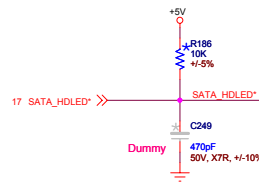
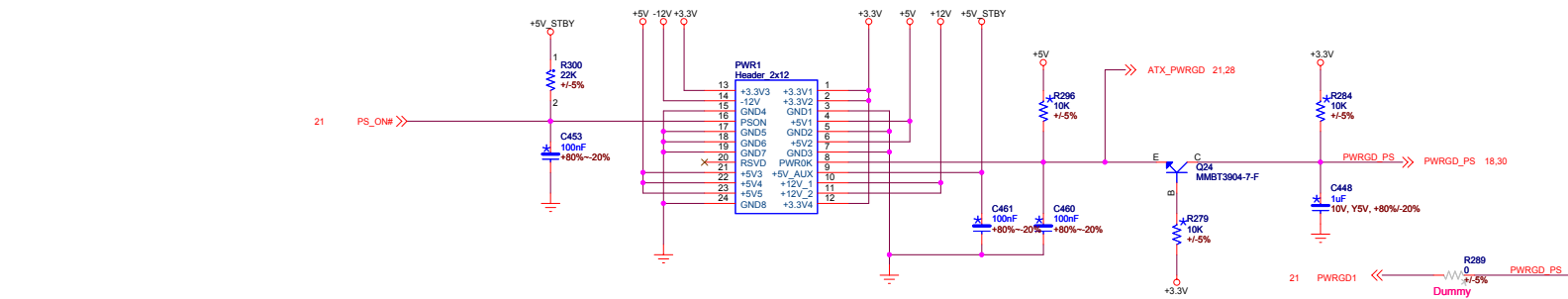
FOXCONN PCEG

File		
Hardware Monitor / Over Volt		
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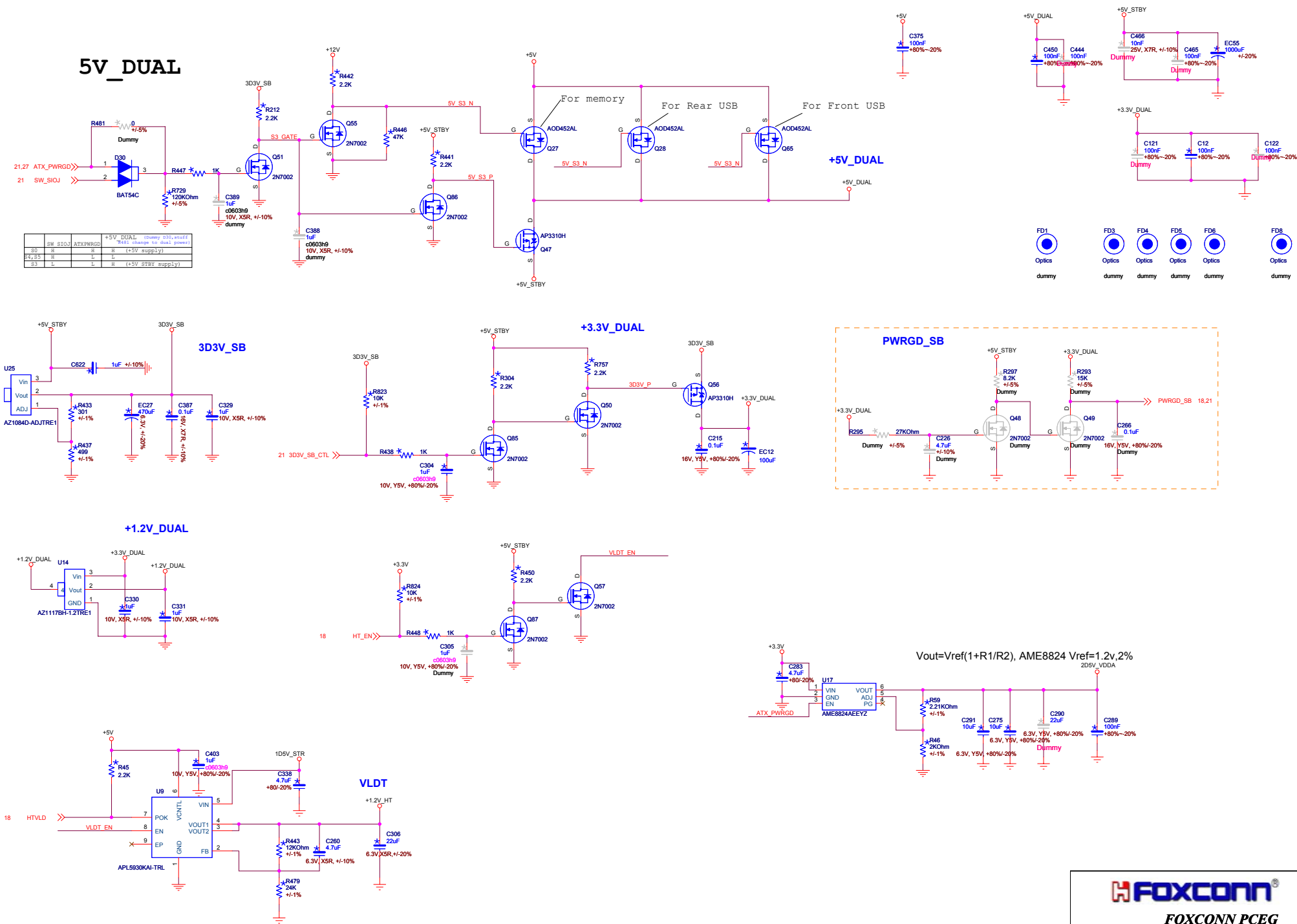
Connect to rear LAN/USB port



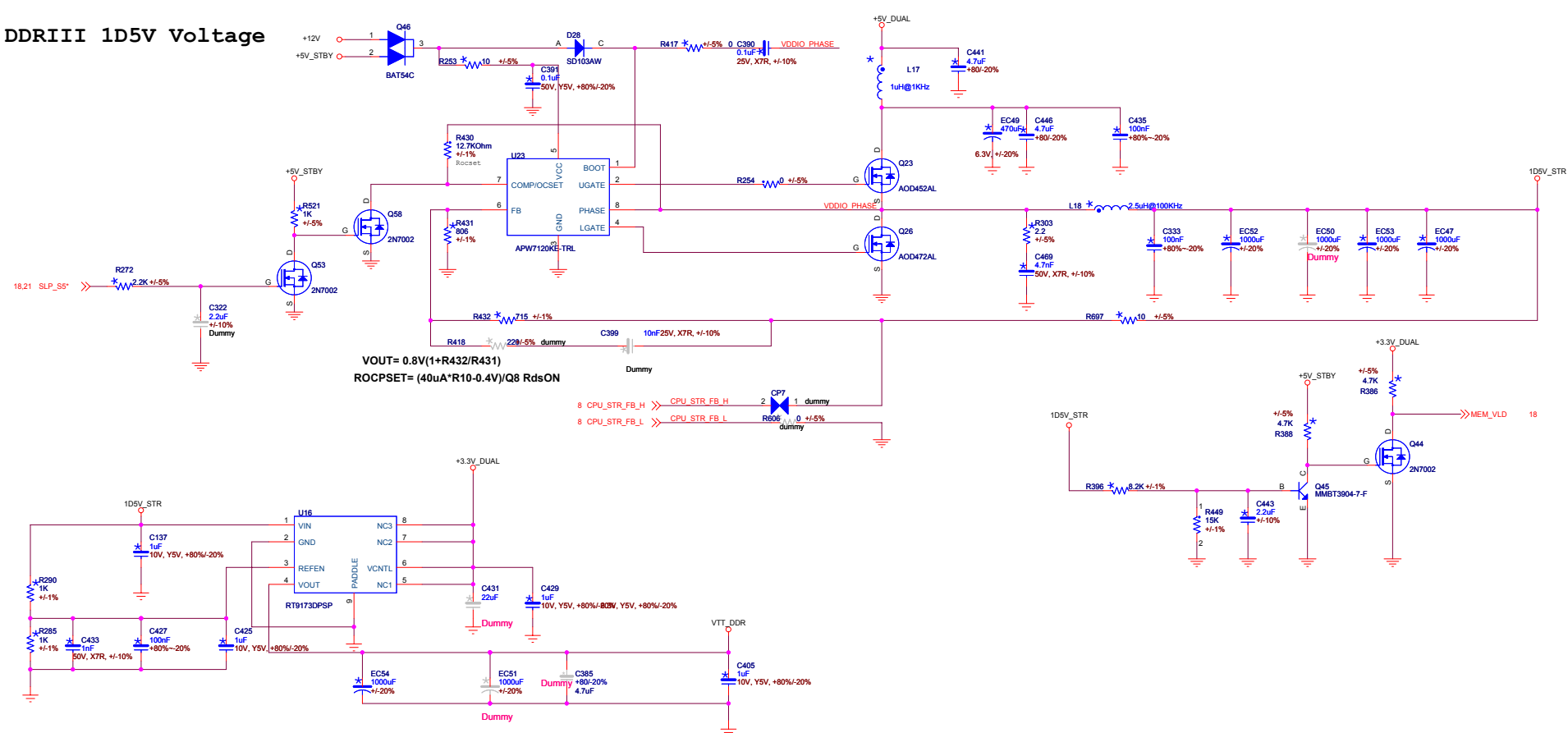




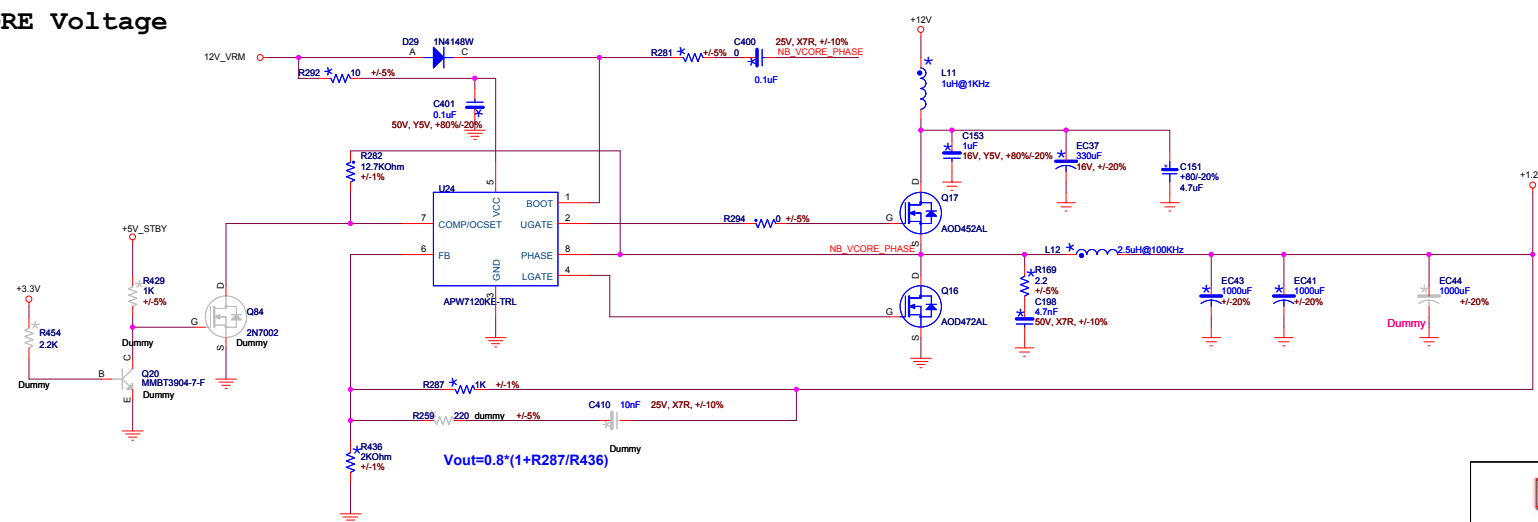
	SW SIOJ	ATXPWRGD	+5V DUAL (Dummy D30,stuff E481 change to dual power)
S0	H	H	H (+5V supply)
S4,S5	H	L	L
S3	L	L	H (+5V STBY supply)



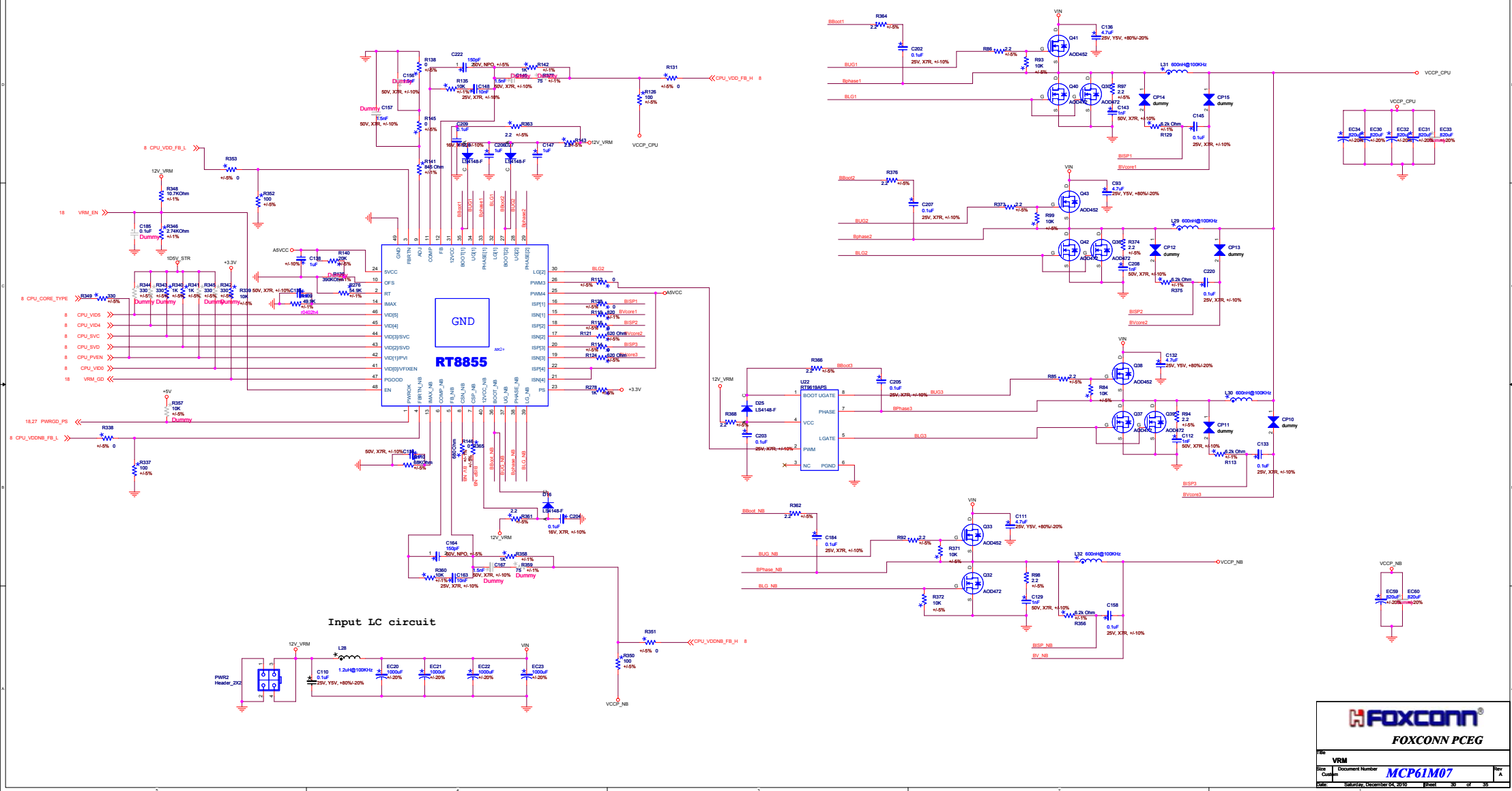
DDRIII 1D5V Voltage

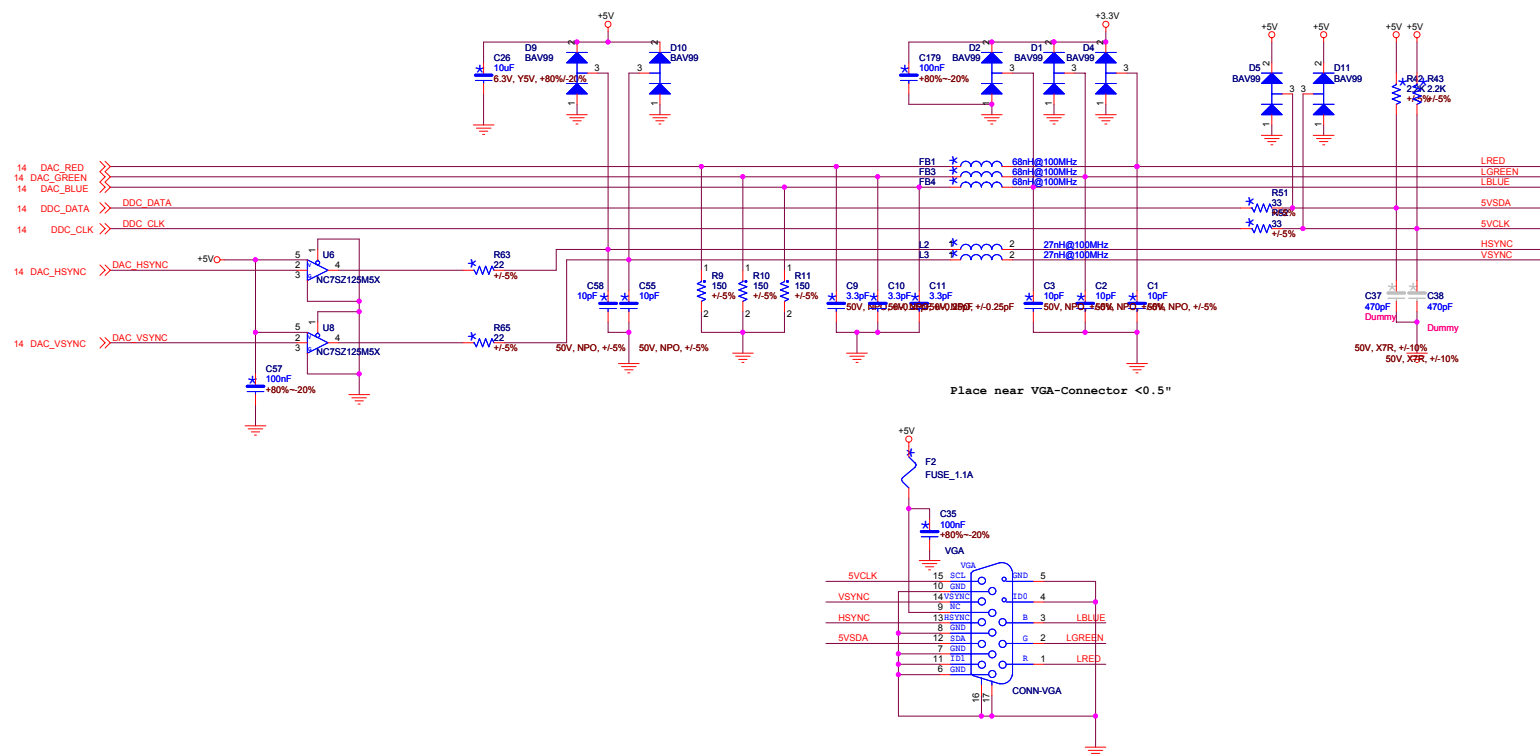


1D2V CORE Voltage

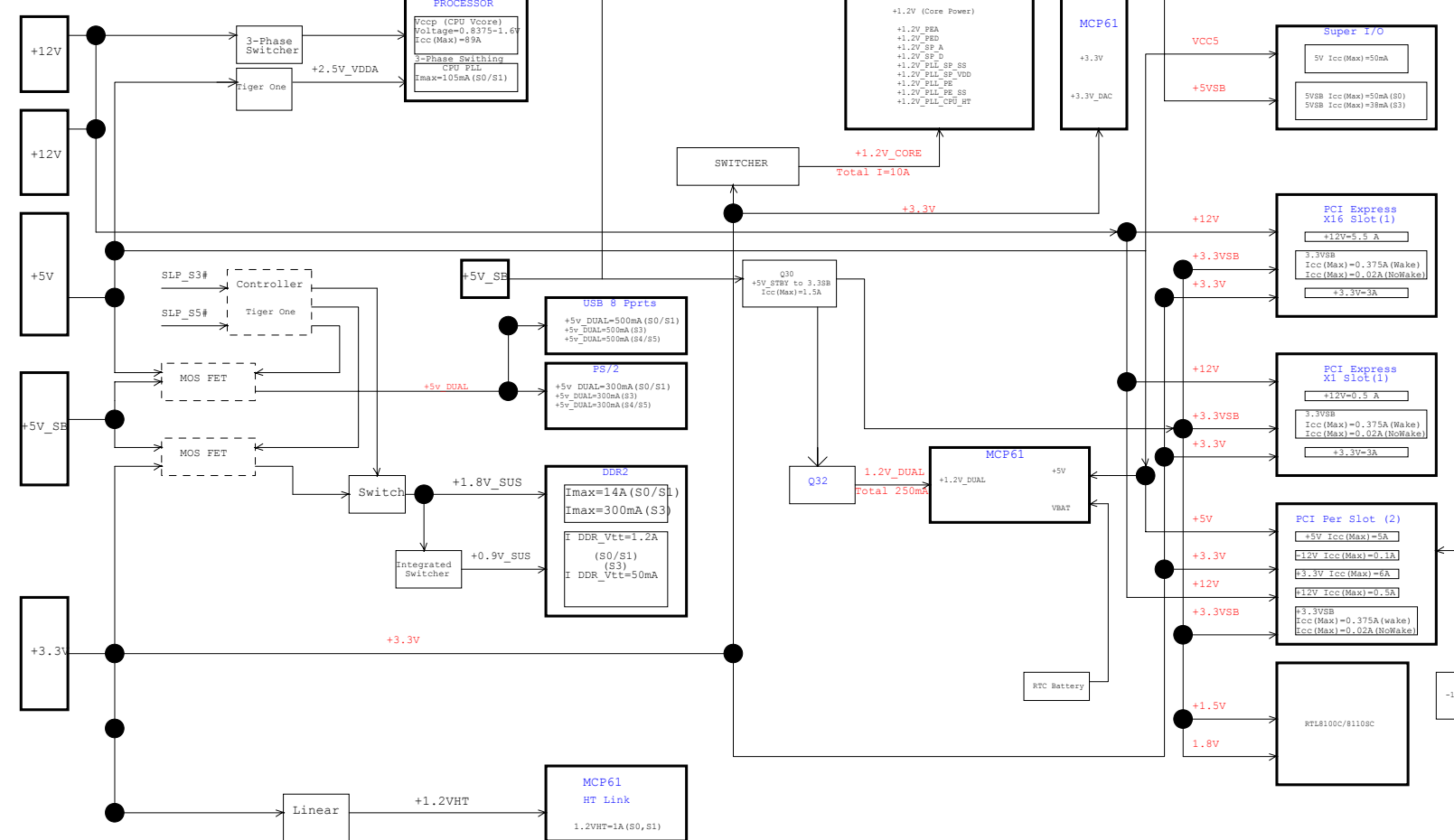
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MCP CORE +1.2V			
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ATX PowerSupply



6/18 : 1,USB: 0 ohm R change to 0 ohm RN, 4pin Bead change to 8pin Bead; 2, BIOS,LPC change to SPI . 3, LAN change to AC131 + PCI LAN :RTL8100C/8110SC,

6/20 : 1,LAN CLK 走南橋, Dummy 外部晶振, Remove AC131 PHY LAN: 2, R623, R624 16.9 ohm 改為15 ohm : 3, USB Fuse 2.6A 替代2個1.5A : 4, F_Audio 75 ohm /22k ohm 電阻閤並成排阻

6/21 : 1. LAN 49.9 ohm 電阻閤並成排阻49.9 ohm: 2. R388 去掉, SIO部分有串接10ohm 電阻: 3, Dummy C332,C301,C310,C300,C320,C290,C347.

6/22 : 1,去掉R355, R829, R830, R832: 2. dummy C572 : 3. ADD C2136 0.1uF to GMII_RXCLK, R57 change to 330K;

6/29: 1, Add 75 ohm damping resistance for Audio ; 2,F_Audio detect pin connect to sense_B pin of CODEC; 3, ADD prtction Diode to COM port .

7/2 : 1,remove L99,L100,L102; Change heatsink with foxconn log; 2, Remove RN122 .

7/3: 1, ADD C 956(4.7uF/805) to 3.3v_Dual ; 2, dummy EC83 (5V_SB); 3, Remove C412, C352,C354;

7/5: 1, change C374,C378 to 0.1uF/0603; 2, dummy C157,C244,C267,C193,C286,C645,C199,C247,C312,C315,C325,C327,C328; 3, Remove C385,C386,C407,C865,C387,C866;

7/7: 1, Change D6,D7,D8,D17,D20,D23,D47 footprint to so80h16; 2, change RN45,RN46 from 8p4r0603 to 8p4r0402 ; 3, add EC106 100uF to +1.2V_dual, dummy EC105 ; 4, Q129,Q131 change to AP15N03GH;

7/9: 1, GPIO PIN: Board ID Select. add R363,R364,R365; Default add R363; 2, Remove C808,C809,C810,C811,C821,C89,C806,C807,C156,C268,C970, C52,C74,C49,C976,C61,C83,C73,C76,C72,EC66 ; 3, add EC50, dummy EC14;

7/11 : 1, add EC107 to auduo 12 V power, C733 change to 10uF, add L28 to audio power DVDD ; 2, ADD EC60 to 3.3V_DUAL for LAN Power ,default dumy ; 3, add R368, R371 to modify the SPI clock; 4, Remove C7,C8,C11,R517,R530,R536 (Audio).

- 8/16 : 1 .L12/L20 change to 1uH/1kHz
- 2 .EC39/38 change to 680uF
- 3 . add R501/502 for CD-IN
- 4 .PCI SLOT IDSEL
- 5 .add EC103 (1.2V OUTPUT)
- 6 .EC35/37 change to 470uF
- 7 . add EC104/105
- 8 .C392/396 change to 22p
- 9 .Retention Module for CPU change HH P/N
- 10 .PEA POWER del copper,FB
- 11 .R83 dummy,and add thermal trip to SIO through level shift
- 12 .C238 change to 220pF
- 13 .R163 change to 680R
- 14 .SATA2,SATA3 change each other
- 15 .Del R77/72/133
- 16 .R262 change to 1.1k
- 17 .C495 change to 10uF and reserved
- 18 .C496 reserved

- 9/12 : 1 .USB_OC add R550/R51/R552/R553 for 3.3V
- 2 .Exchange usb3/4;
- 2 .change C385/C391/C392/C396 from 0603 to 0402

- 9/19 : 1 .change c392/c396 22pf to 24pf

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



FOXCONN PCEG

CHANGE LIST		
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SD Ram (168 Pins, 3.3V) Pin Details

Supply:- 6,18,26,40,41 Ground:- 1,12,23,32 Data:- 2,3,4,4,7,8 Address:- 33,34,35,36,37

DDR-1 Ram (184 Pins, 2.5V) Pin Details

Supply:- 7,15,22,30,46 Ground:- 3,11,26,50 Data:- 2,4,6,12,13 Address:- 32,37,41,43,48
WE:- 63 CAS:- 65 RAS:- 154 SM DATA:- 91 SMCLOCK:- 92 BA:- 52,59
SPDVDD:- 184 Vref:- 1 CS:- 157,158 CKE:- 21,211 DCLK:- 16,17,137,138

DDR-2 Ram (240 pins, 1.8V) Pin Details

Supply:- 53,59,64 Ground:- 2,5,11,14 Data:- 3,4,9,10,12,13 Address:- 57,58,60,61
WE:- 73 CAS:- 74 RAS:- 192 SM DATA:- 119 SMCLOCK:- 120 BA:- 71,190
SPDVDD:- 238 Vref:- 1 CS:- 76,193 CKE:- 52,171 DCLK:- 221,220,138

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DDR-3 Ram (240 Pins, 1.5V) Pin Details

Supply:- 51,54,57,60,62 Ground:- 2,5,8,11,14 Data:- 3,4,6,7,9,10 Address:- 55,56,58,59,61
WE:- 73 CAS:- 74 RAS:- 192 SM DATA:- 238 SMCLOCK:- 118 BA:- 82,190
SPDVDD:- 236 Vref:- 1 CS:- 193 CKE:- 50,93,94 DCLK:- 184,185

VTT:- 120,240

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